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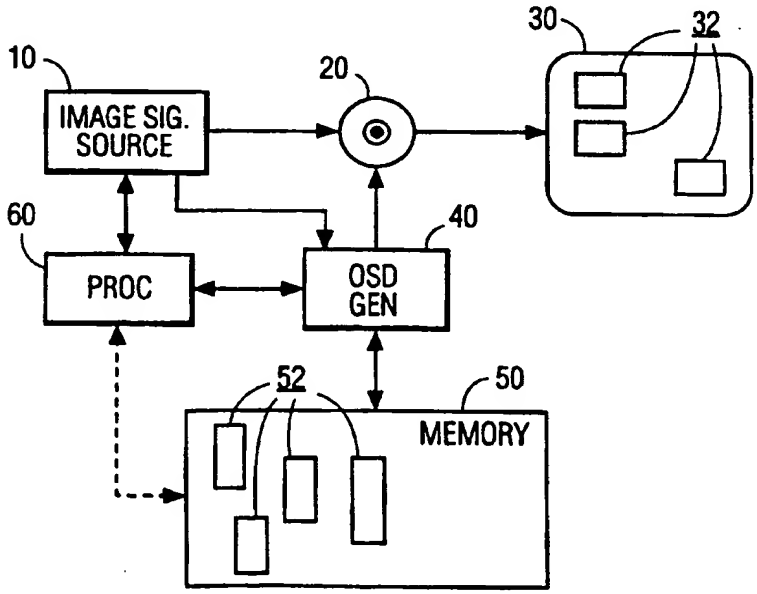
(54) Title: LINKED LIST STRUCTURE ONSCREEN DISPLAY

(57) Abstract

An onscreen display (OSD) system includes a source (10) of a background image representative signal. An OSD (50) memory stores a sequence of blocks, each block containing data representing an OSD. Each block also includes a pointer to a next block in the sequence. An OSD generator (40) retrieves the blocks from the OSD memory in order, and generates an OSD image representative signal from the OSD representative data. A signal combiner (20) combines the background image representative signal and the OSD image represntative signal.



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# LINKED LIST STRUCTURE ONSCREEN DISPLAY

## FIELD OF THE INVENTION

The present invention relates to an onscreen display architecture, for use in television receivers, which stores display representative data in a linked list.

## BACKGROUND OF THE INVENTION

Current television receivers often use onscreen displays (OSDs) to convey information to a user. For example, in television sets, an OSD displays the current channel when a user changes the channel; or displays a bar graphically illustrating the current volume of the television set when the user adjusts the volume. In video cassette recorders, an OSD is used to assist the user in entering schedule information for unattended recording. It has been proposed to provide animated OSDs to further enhance the user interface.

Current OSD display systems use a known bitmapped architecture in which the OSD image is considered to be an array of picture elements (pixels) arranged as N rows, each row containing M pixels arranged in columns. Each pixel in the OSD array can assume one of a predetermined number of colors. Data representing the image in the OSD pixel array is stored in a memory, termed an OSD memory in the remainder of this application, which is arranged in a corresponding array of N rows, each row containing M pixelrepresentative words. In a blackandwhite display, the pixelrepresentative words are 1 bit wide representing either black or white. In monochrome displays, each pixel representative word contains a plurality of bits representing the gray scale level of that pixel. Color pixels are represented by three sets of color level bits, one set for each of the primary colors: red, green, and blue. Alternatively, each pixel representative word can represent one of a predetermined number of colors selected from a palette. Most current OSDs use the palette technique.

In current OSD display systems, the image data defining the contents of the OSDs to be displayed for the next field, and the new palette and other control data, are stored (in the

format described above) in the OSD memory during the vertical blanking interval (VBI). As the television receiver begins to scan the visible portion of the raster, line and pixel counters maintain the location in the raster currently being scanned, and if an OSD is specified for that area, the OSD image data from the OSD memory is overlaid on the received video signal. For example, the OSD data could replace the received video signal, or could be combined with the video signal in some manner, as is well known. During the readout times for the OSD memory, the OSD memory must produce data with a relatively high bandwidth. This requirement has been met by the use of a specially designed video read/write memory (VRAM) which can serially shift a wide data output word in a single memory access time. This, in turn, requires that the data for the OSDs be located contiguously in the memory to minimize addressing and access time.

Animation is produced by displaying a time sequence of OSDs for a single location on the screen in which the image of each OSD is slightly different from the preceding one. For example, an animation of a door opening may start with an OSD of a door in a closed position, followed by an OSD with the door onequarter open, then with the door half open, then threequarters open, and finally completely open. If the OSD images in the animation are relatively simple then data representing each one may be updated during the vertical blanking interval. However, if the OSD is complex, there will be no time for such updating. An OSD architecture which facilitates animated OSD is desirable.

## BRIEF SUMMARY OF THE INVENTION

In accordance with principles of the present invention, an onscreen display (OSD) system includes a source of a background image representative signal. An OSD memory stores a sequence of blocks, each block containing data representing an OSD. Each block also includes a pointer to a next block in the sequence. An OSD generator retrieves the blocks from the OSD memory in order, and generates an OSD image representative signal from the OSD representative data. A signal combiner

combines the background image representative signal and the OSD image representative signal.

An OSD according to the present invention does not require that the OSD information be written in the OSD memory in a single contiguous block. Instead, because each block contains a pointer to the next block in the sequence, the blocks may be stored in arbitrary noncontiguous locations in the OSD memory. This obviates the requirement that the OSD data be completely written into the memory during the VBI. Instead, OSD blocks may be written into the OSD memory at any time, and only the pointers updated during the VBI. This permits more complex changes in the OSDs from field to field, facilitating animated OSDs.

## BRIEF DESCRIPTION OF THE DRAWING

In the drawing:

FIGURE 1 is a block diagram of a portion of a television signal receiver including an onscreen display system according to the present invention; and

FIGURE 2 is a memory layout diagram of information in the OSD memory of the onscreen display system illustrated in FIGURE 1.

## DETAILED DESCRIPTION

FIGURE 1 is a block diagram of a portion of a television signal receiver including an onscreen display system according to the present invention. FIGURE 1 illustrates only those elements of such a television receiver which are necessary to understand the invention. One skilled in the art will understand what other elements are required, and how to design, implement and interconnect such elements with the illustrated elements.

In FIGURE 1, an image signal source 10 produces an image representative signal. An image signal output terminal of the image signal source 10 is coupled to a first input terminal of a signal combiner 20. An output terminal of the signal combiner 20 is coupled to an input terminal of a display device 30. An onscreen display (OSD) generator 40 has a bidirectional terminal coupled to an OSD memory 50, and an output terminal coupled to a second input terminal of the signal combiner 20. A status

output terminal of the image signal source 10 is coupled to a corresponding input terminal of the OSD generator 40. A control processor 60 includes a first bidirectional control terminal coupled to the image signal source 10, and a second bidirectional control terminal coupled to the OSD generator 40.

In operation, the image signal source 10 may be a television receiver front end of known design for reception of an offair, cable or satellite transmitted signal, or may be the playback mechanism of a video cassette recorder or videodisc, also of known design. The control processor 60 controls the image signal source 10, for example, to tune a channel or select a prerecorded program on a videodisc or video cassette recorder. The image signal source 10 produces a signal representing the image the viewer desires to watch. The image representative signal may be a standard (e.g. NTSC) video signal, or any other image representative signal, such as the RGB drive signals for a kinescope in the television display device 30. This signal is passed to the display device 30 through the signal combiner 20. The display device 30 produces a visible image for the viewer, and may be a television receiver or monitor, including a picture tube, of known design. The display device 30 displays the image represented by that image representative signal for the viewer in the entire screen represented by the rounded rectangle in FIGURE 1.

The control processor 60 also stores in the OSD memory 50 a plurality 52 of blocks, to be described in more detail later, each of which defines an onscreen display image in the bitmapped/palette format described above. The control processor 60 writes these blocks 52 into arbitrary locations in the OSD memory 50 using the OSD generator 40 as a write control circuit, in a known manner. In an alternative embodiment, the control processor 60 may write the blocks into the OSD memory 50 directly, as indicated in phantom in FIGURE 1. The control processor 60 also provides the OSD generator 40 with the location in the OSD memory 50 of the first one of these blocks 52 to be displayed. The OSD generator 40 reads the block 52 at this

location to determine the row and pixel where the OSD image represented by this block will be located on the image displayed by the display device 30.

The image signal source 10 provides to the OSD generator 40, via signals at its status output terminal, the line and pixel currently being scanned. The OSD generator 40 monitors the line and pixel currently being scanned. When the scan reaches the location to be filled by the OSD represented by the first block, the OSD generator 40 retrieves the data from the block 52 representing that OSD, and generates an image representative signal representing that OSD from the bitmapped/palette data, in a known manner. This OSD image representative data from the OSD generator 40 is then supplied to the signal combiner 20 to be combined with the received or reproduced image from the image signal source 10.

The signal combiner 20 operates in a known manner to combine the OSD image representative signal with the received or reproduced image representative signal to produce an image on the display device 30 including the received or reproduced image as the background image, with the OSDs 32 positioned within that background image. For example, the signal combiner 20 may replace the background image with the OSD image, i.e. the signal combiner operates as a simple switch. Alternatively, the signal combiner 20 may mix the OSD image and the background image in a predetermined proportion. Or one color of the palette of colors defining the OSD image may represent 'transparent', and when that color is produced by the OSD generator 40, the background image is allowed to show through the OSD image, otherwise the OSD image overlays the background image.

In addition, it is possible for the OSD representative information in the block 52 in the OSD memory 50 to control the operation of the signal combiner 20. For example, the OSD generator 40 may condition the signal combiner 20 to vary the proportion of the background image representative signal to the OSD image representative signal in response to data stored in the block 52 in the OSD memory 50 defining that OSD. For example,

the proportion may be varied from 0% (i.e. the OSD image opaquely overlays the background image), to 20% (i.e. the background image is barely visible through the OSD image, to 80% (i.e. the OSD image is barely visible through the background image), to 100% (i.e. the OSD image is invisible).

The OSD generator 40 may also condition the signal combiner 20 to selectively enable or disable the 'transparent' color operation in response to data stored in the block 52 in the OSD memory 50 for that OSD. Further, it is possible to include data with each entry in the palette in each block 52 which defines whether the color defined by this palette entry is to be mixed with, or to overlay, the background image signal.

FIGURE 2 is a memory layout diagram of information in the OSD memory 50 of the onscreen display system illustrated in FIGURE 1. In FIGURE 2, the OSD memory 50 is illustrated as a rectangle and the layout of the blocks 52 of OSD data within the OSD memory 50 is illustrated by other rectangles within the OSD memory 50. The corresponding display 30, displaying a background image and three OSD images 32, is also illustrated in FIGURE 2. In addition, a pointer to the location of the first OSD block in the OSD memory 50 is contained in a data store 42. Data store 42 may also be a location within the OSD memory 50, or a hardware register separate from the OSD memory 50.

Specifically, there are five OSD blocks stored at arbitrary locations in the OSD memory 50. Block 1, 52(1), corresponds to OSD 1; block 2, 52(2), corresponds to OSD 2; block 3A, 52(3A), corresponds to OSD 3; and block 4, 52(4) corresponds to an OSD not illustrated on the display 30 for the sake of simplicity in the figure. Each block 52 includes a header, followed by the bitmapped/palette data describing the OSD image represented by this block. In FIGURE 2, only blocks 1 and 2, 52(1) and 52(2), respectively, are shown in detail, but all blocks 52 have similar structure. The header contains data, denoted LOC in FIGURE 2, representing the line and pixel of the location of the OSD image on the display 30. The header also contains a pointer, denoted PTR in FIGURE 2, to the location in the OSD memory 50 of

the block containing data defining the next OSD to be displayed on display 30. The header also contains other data, represented by an ellipsis, related to the OSD represented by this block, e.g. a mixing proportion. The bitmapped/palette data representing the OSD image, denoted IMAGE DATA in FIGURE 2, is arranged in a known manner in the remainder of the block 52.

In general operation, the control processor 60 (of FIGURE 1) generates and stores the blocks 52 in the OSD memory 50, then, during the VBI, sets the start pointer 42 and all the pointers, PTR, in the blocks 52 to form a sequence of blocks 52, representing a sequence of OSDs 32. During the active portion of the scan, the OSD generator 40 retrieves the previously stored data in the sequence of blocks 52 from the OSD memory 50 and generates an OSD image representative signal which is combined with the background image signal from the image signal source 10 in the signal combiner 20 to form a signal representing the image on the display 30 with the OSDs 32.

For example, in FIGURE 2, blocks 1, 2, 3A, and 4 have been previously written into the OSD memory 50 by the control processor 60 before the beginning of the current field. As can be seen from FIGURE 2, the blocks 52 need not be contiguous. The header of each block contains the location on the display 30 of the OSD 32 represented by that block. This is indicated in FIGURE 2 by straight arrows from the display location pointer LOC in block 1, 52(1), to the location on the display 30 of OSD 1, from the LOC pointer in block 2 to OSD 2, and from the LOC pointer in block 3A to OSD 3..

During the VBI of the current field, the processor 60 stores the location of block 1 in the start pointer 42, the location of block 2 in the pointer PTR of block 1, the location of block 3A in the pointer PTR of block 2, and the location of block 4 in the pointer PTR of block 3A (all represented in FIGURE 2 by curved arrows from the location in the OSD memory 50 containing the pointer to the location pointed to by that pointer), and an outofrange value (i.e. a row and/or pixel value which is not within the display area of the display 30) in the pointer of block 4. This

process is a relatively fast one involving only a few memory accesses, even for a display 30 containing a large number of complex OSDs 32.

At the beginning of the active portion of the current field, the OSD generator 40 retrieves block 1, 52(1), pointed to by the start pointer 42, and reads the header. From the header, the OSD generator 40 extracts the pointer LOC to the row and pixel location of OSD 1 on the display 30, and the palette for OSD 1 stored in the image data portion of block 1 52(1). Then the OSD controller 40 begins to monitor the row and pixel currently being scanned, as supplied by the image signal source 10. When the row and pixel of OSD 1 is reached, the OSD generator 40 supplies the OSD 1 image data from block 1, 52(1), to the signal combiner 20, where it is combined with the background image representative signal, all in a known manner.

When the display of OSD 1 is completed, the pointer PTR from block 1, pointing to block 2, 52(2), is extracted from the header information. Using this pointer to locate block 2, 52(2), the image data for OSD 2 is then retrieved from the OSD memory 50, and processed in the same manner described above for block 1, 52(1). When OSD 2 has been displayed, OSD 3, represented by block 3A, 52(3A), and the OSD (not shown) represented by block 4, 52(4), are then displayed, in that order. When OSD 4, represented by block 4, 52(4), has been displayed, the pointer from the header of block 4, 52(4), is extracted. Because it is an outofrange value, this indicates to the OSD generator 40 that there are no more OSDs to be displayed in this field, and the OSD generator 40 stops processing blocks 52.

In FIGURE 2, OSD 3 may be an animated OSD, which in the illustrated embodiment has two images which are alternated rapidly to create the animation effect. It is also possible to have more than two images (i.e. 3A, 3B, 3C, 3D, etc.), which are displayed in order, in the animation. The control processor 60 can write blocks 52 into the OSD memory 50 defining all of the different images of OSD 3 to be displayed in the animation in advance. During the field described above, the first image

(defined by block 3A, 52(3A)) of the OSD 3 animation was displayed. During the VBI of the next field, the control processor 60 writes the location of block 1, 52(1), into the start pointer 42; the location of block 2, 52(2), into the pointer PTR of block 1, 52(1); the location of block 3B, 52(3B), (instead of block 3A, 52(3A)) into the pointer PTR of block 2, 52(2) (as illustrated in phantom in FIGURE 2); and the location of block 4, 52(4), into the pointer PTR of block 3B, 52(3B) (also as illustrated in phantom in FIGURE 2). During this field, the second image of the OSD 3 animation is displayed. For the next field, the OSD 3 image represented by block 3A, 52(3A), is again displayed in OSD 3 by changing the pointer PTR in block 2, 52(2) to point to the location of block 3A, 52(3A) again during the VBI. If more than two images were part of the animation, each would be displayed in its turn by placing the location of its block 52(3*) into the pointer PTR of block 2, 52(2).

Alternatively, OSD 3 may be an OSD displaying information which changes relatively rapidly. During the active portion of a field, a new value is determined by the control processor 60, which generates a new OSD image representing this new value and stores the image representative data in block 3B. During the VBI, this newly generated OSD 3 image is linked into the sequence of blocks defining the OSDs, as illustrated in phantom in FIGURE 2, by placing its location in the OSD memory 50 into the pointer PTR of block 2, 52(2). The block 52(3A) containing the image displaying the previous value of the information may then be released and used for other purposes.

Because the blocks defining the OSD images need not be contiguous, as in the prior art, the control processor 60 may generate a complete series of image representative blocks 52 in advance, such as for animation, or a new image representative block representing a new value of information at any time in the scan. During the VBI, the next image in the animation, or the newly generated OSD image is simply linked into the sequence of OSDs by changing only the pointers in the OSD image blocks 52. The time spent in updating the start pointer 42 and the pointers

PTRs in the blocks 52 is minimal, and a relatively large number of OSDs of arbitrary size, and which change relatively rapidly, may be maintained in an OSD display system according to the present invention.

The illustrated embodiment included a single start pointer 42. But one skilled in the art will understand that to obtain the maximum vertical resolution in an interlaced display system, respectively different OSD blocks 52 may be used for odd and even fields for the same OSD 32. In such an embodiment, two start pointer data stores (corresponding to data store 42) may be maintained, one for odd fields, and one for even fields, and each pointing to the start of respectively different sequences of OSD image data blocks 52 stored in the OSD memory 50 by the control processor 60. During odd fields, the sequence pointed to by the odd field start pointer is processed, and during even fields, the sequence pointed to by the even field start pointer is processed. Alternatively, two different sequences (an odd field sequence, and an even field sequence) of data blocks 52 may be maintained in the OSD memory 50 by the control processor 60, as above, and the contents of the single start pointer data store 42 changed by the control processor 60 so that the image representative signals represented by the odd field sequence are produced during odd fields, and those represented by the even field sequence of OSD blocks 52 are produced during even fields.

## CLAIMS

1. An onscreen display (OSD) system, comprising:

a source (10) of a background image representative signal;

an OSD memory (50), for storing in arbitrary locations a sequential plurality of blocks, each block containing data representing an OSD image and a pointer to a next block in the sequence;

an OSD generator (40), for sequentially retrieving the sequential plurality of blocks from the OSD memory, and generating an OSD image representative signal in response to the OSD image representative data in each retrieved block; and

a signal combiner (20), for combining the background image representative signal and the OSD image representative signal.

2. The system of claim 1 wherein:

the background image signal source (10) further comprises circuitry for producing a signal representing the location in the background image currently being produced by the background image signal source;

each one of the sequential plurality of blocks further contains data representing a location in the background image at which the image represented by the OSD image representative data stored in the one of the sequential plurality of blocks is to be displayed; and

the OSD generator (40) comprises circuitry, responsive to the location representative signal from the background image signal source, for monitoring the location in the background image currently being produced by the background image signal source, and generating the OSD image representative signal corresponding to the OSD image representative data in the retrieved block when the location currently being produced by the background image signal source is the location in the background image at which the OSD image is to be displayed.

3. The system of claim 1 further comprising a control processor (60), coupled to the OSD memory, for generating and storing the sequential plurality of blocks in the OSD memory.

4. The system of claim 3 wherein:

the background image representative signal includes repetitive vertical blanking intervals; and

the processor (60) comprises circuitry for storing the blocks in the OSD memory (50) at any time, and storing the respective pointers to the next block in each of the sequential plurality of blocks during the vertical blanking interval.

5. The system of claim 1 wherein the OSD generator comprises:

a starting pointer data store (42), for storing a location in the OSD memory of a first block in the sequential plurality of blocks;

circuitry for retrieving the first block of the sequential plurality of blocks by accessing the OSD memory at the location pointed to by the starting pointer data store;

circuitry for generating the OSD image representative signal responsive to the OSD image representative data in the retrieved block; and

circuitry for extracting the pointer to the next block in the sequential plurality of blocks from the retrieved block.

6. The system of claim 5 wherein the OSD generator further comprises circuitry for sequentially:

retrieving the next block of the sequential plurality of blocks by accessing the OSD memory at the location pointed to by the pointer to the next block in the sequential plurality of blocks;

circuitry for generating the OSD image representative signal responsive to the OSD image representative data in the retrieved block; and

circuitry for extracting the pointer to the next block in the sequential plurality of blocks from the retrieved block.

7. The system of claim 5 further comprising a control processor, coupled to the OSD generator and the OSD memory, for generating and storing the sequential plurality of blocks in the OSD memory, and the location of the first one of the sequential plurality of blocks in the starting pointer data store.

8. The system of claim 5 wherein the starting pointer data store is a location in the OSD memory.

9. The system of claim 5 wherein the starting pointer data store is a register.

10. The system of claim 1 wherein the background image representative signal source comprises television signal receiving circuitry.

11. The system of claim 1 wherein the background image representative signal source comprises television signal reproduction circuitry.

12. In an onscreen display (OSD) system, comprising a source (10) of a background image representative signal and an OSD memory, a method for displaying a plurality of onscreen display images, comprising the steps of:

storing a plurality of blocks of data in the OSD memory respectively corresponding to the plurality of onscreen display images;

forming a sequence of memory blocks, by storing within each block, a pointer to the next block in the sequence,

retrieving data from each block in the sequence and generating an OSD image representative signal corresponding to the retrieved data;

combining the OSD image representative signal with the background image representative signal; and

repeating the retrieving and combining steps sequentially for each block in the sequence of memory blocks.

13. The method of claim 12 wherein:

the repeating step comprises the step of retrieving the pointer to the next block in the sequence; and

the retrieving step comprises the step of retrieving the block from the location in the OSD memory pointed to by the retrieved pointer to the next block in the sequence.

14. The method of claim 12 wherein the background image representative signal includes repetitive vertical blanking intervals, and the step of forming a sequence of memory blocks comprises, before the step of storing the pointer, the step of waiting until the vertical blanking interval.

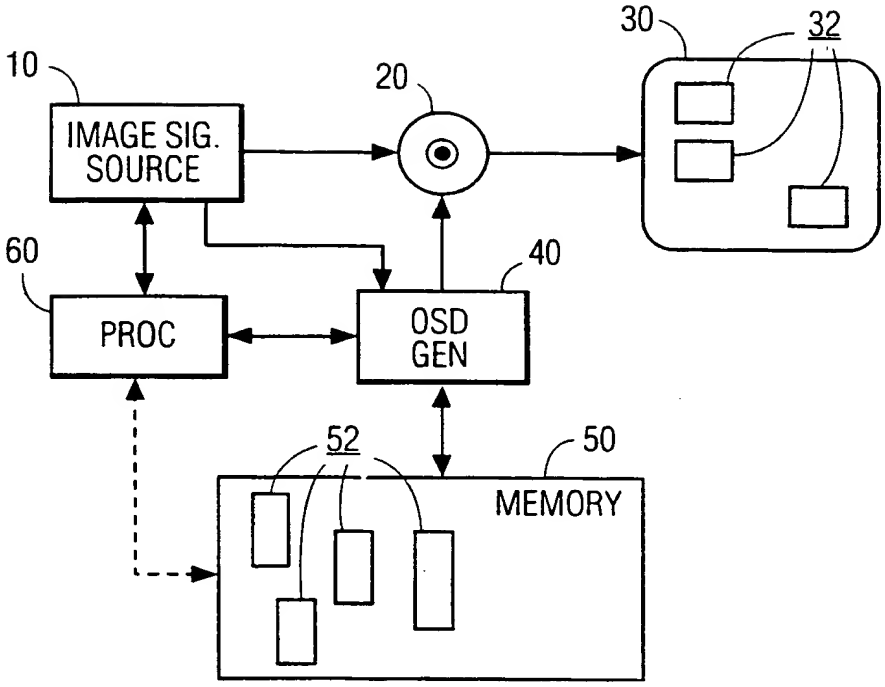


FIG. 1

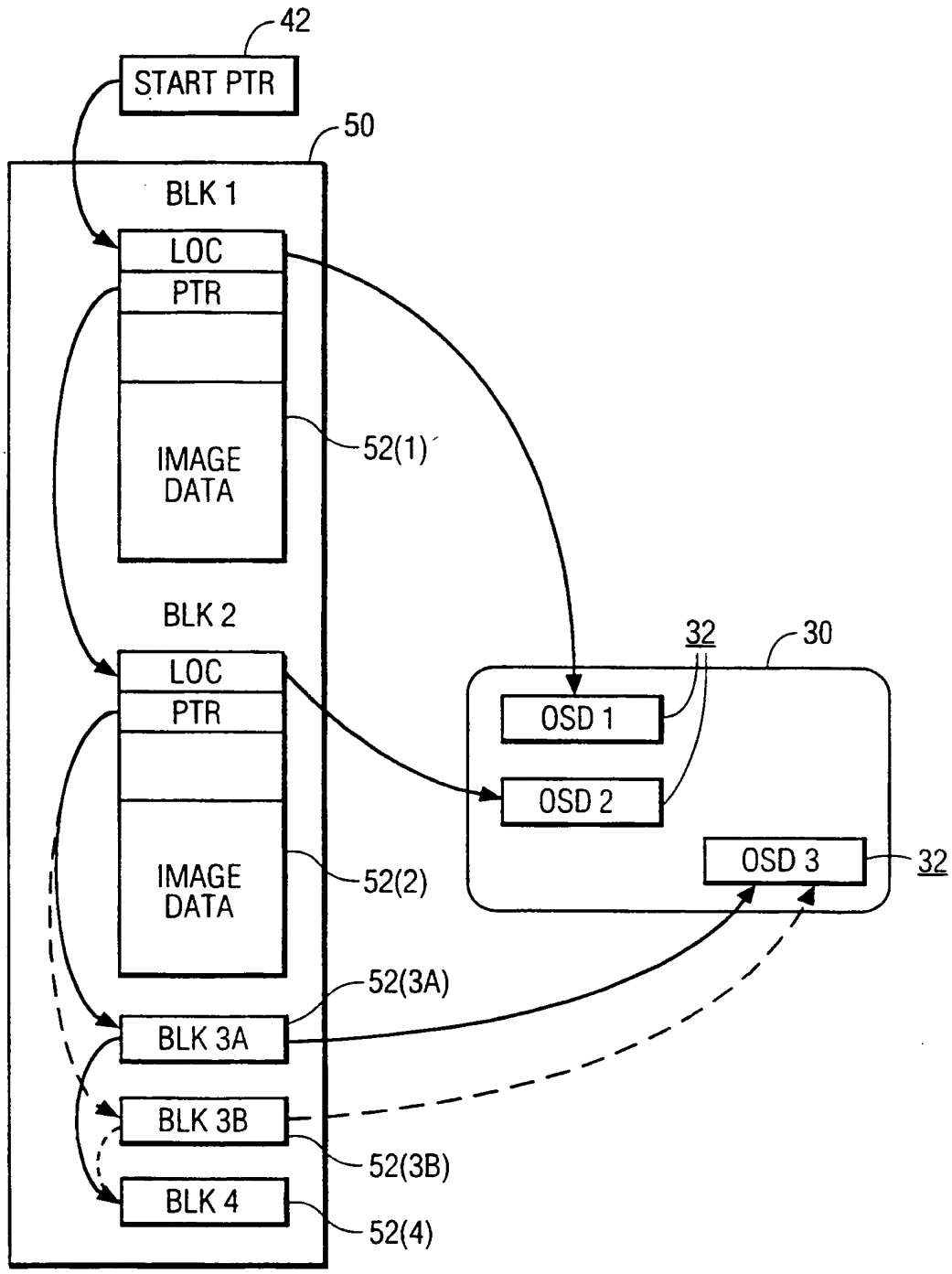
42
START PTR
50
BLK 1
LOC
PTR
IMAGE DATA
52(1)
BLK 2
LOC
PTR
IMAGE DATA
52(2)
32
30
OSD 1
OSD 2
OSD 3
32
52(3A)
BLK 3A
BLK 3B
52(3B)
BLK 4
52(4)

FIG. 2

# INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 96/12164

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04N5/445 G09G1/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04N G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | EP,A,0 222 920 (ISS KK) 27 May 1987<br>see the whole document<br>--- | 1,12 |
| A | GB,A,2 104 760 (BALLY MFG CORP) 9 March 1983<br>see abstract<br>see page 1, line 99 - page 2, line 47; figure 1<br>--- | 1,2,12 |
| A | US,A,4 203 107 (LOVERCHECK LAWRENCE R) 13 May 1980<br>see column 2, line 45 - line 66<br>see abstract<br>--- | 1,5,12, 13 |
| A | US,A,5 296 918 (KIM JAE-CHUL) 22 March 1994<br>see column 2, line 15 - line 32; figure 1<br>see column 1, line 44 - line 68<br>----- | 1,12 |

☐ Further documents are listed in the continuation of box C.

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|---|---|
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